Ahmed S. Emara, Ph.D., P.Eng.

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Industrial Experience

Staff Analog & Mixed-Signal Circuit Design Engineer, **Marell Technology**, Toronto, ON, Canada (Jan 2025 – Present)

- Designing and verifying **7 + 8 bits fully binary and segmented (binary + thermometer) calibration DACs** used in die-to-die (D2D) interface IP. This includes single-ended and differential-ended implementations.
- Designing and verifying the **R_X AFE sideband** module which includes **resistive ladder DAC** and an **Auto Zeroing Comparator**. used in die-to-die (D2D) interface IP.
- Performing **Design for Manufacturability (DFM)** simulations for circuit blocks in die-to-die (D2D) interface, including Electromigration (EM), IR drop, Reliability, Aging, and Self-Heating.

Senior Analog & Mixed-Signal Circuit Design Engineer, **Synopsys**, Mississauga, ON, Canada (July 2021 – Jan 2025)

- Designed and verified **AC coupled resistive feedback inverter Duty Cycle Correction (DCC)** circuit in T_X of SerDes, which included a 7-bit current DAC: Freq = 16 GHz, DCC range < 12%, DCC step < 0.2%, D_J < 120 fs, R_J < 70 fs, Power < 10 mW across PVT + MC, PCIe6 compliant (silicon proven results).
- Designed and verified **Clock signal calibration** circuit which included **four-phase generator** and a **static phase interpolator (PI)** circuit in T_X of SerDes: Freq = 8 GHz, Resolution step < 4 ps, 45% < DC < 55%, D_J < 200 fs, R_J < 80 fs, Power < 2 mW across PVT + MC, PCIe6 compliant (silicon proven results).
- Designed and verified **Sub 1V bandgap reference** circuit, which included startup circuit, chopper circuit and RC LPF biased current mirror: V_{BG} = 800 mV, V_{BG} variation = $\pm$ 2%, and I_{ref} = 20 µA, Power = 700 µW across PVT + MC, E112 and PCIe6 compliant (silicon proven results).
- Performed **Design for Manufacturability (DFM)** simulations for different circuits of T_X SerDes, including Electromigration (EM), IR drop and Reliability, Aging, and Self-Heating.

Research Assistant, **Ciena**, Ottawa, ON, Canada - Ph.D. Industrial Partner (Sept 2016 – June 2021)

- Designed, verified and taped-out **segmented ΣΔ current steering DAC**: Resolution = 12-bits, F_S = 20 MHz, DNL < 0.63 LSB, INL < 0.87 LSB, Area = 0.5 mm^2 V_{DD} = 1.2 V.
- Designed and verified **1-Bit, 1st order ΣΔ-ADC** V_{dd}= 1.2 V, SNDR > 50 dB, BW= 20 kHz.
- Conducted literature survey on high-resolution DACs used for calibration and test purposes.

Education

- **McGill University**, Montreal, Quebec, Canada
  Ph.D. in Electrical and Computer Engineering, September 2016 – November 2021
  Thesis Title: Design of Calibration DACs using Periodic Sequences from Sigma-Delta Modulators
  Advisor: Gordon W. Roberts
- **The American University in Cairo (AUC)**, Cairo, Egypt
  M.Sc. in Electronics and Communications Engineering, September 2014 – June 2016
  Thesis Title: On the Production Testing of Analog and Digital Circuits
  Advisor: Hassanein H. Amer, Co-Advisor: Ahmed H. Madian
- **The American University in Cairo (AUC)**, Cairo, Egypt
  B.Sc. in Electronics and Communications Engineering, September 2009 – June 2014
  Graduation Project: Testing of Current Mode Logic (CML) Circuits

U.S. Patent Publication

1- Sadok Aouini, **Ahmed S. Emara**, Gordon W. Roberts, Mahdi Parvizi and Naim Ben-Hamida, "Extremely-Fine Resolution Sub-Ranging Current Mode Digital-Analog-Converter using Sigma-Delta Modulators," U.S. Patent 10,425,099, Filed: November 29, 2018, Granted: September 24, 2019.

Book Chapter Publication

2- S. H. Amer, A. H. Madian, H. Elsayed and **Ahmed S. Emara**, "Theory, Modeling and Design of Memristor-Based Min-Max Circuits," Advances in Memristors, Memristive Devices and Systems, Springer, 2017, 187-205.

Journal Publications

3- Mahmood A. Mohammed, Feras Al-Dirini, **Ahmed S. Emara**, and Gordon W. Roberts. "Design for Slew-Rate in Multi-Stage CMOS OTAs," accepted for publication in IEEE Transactions on Circuits and Systems I: Regular Papers, July 2025.

4- **Ahmed S. Emara**, Denis Romanov, Gordon W. Roberts, Sadok Aouini, Mahdi Parvizi and Naim Ben-Hamida, "An Area-Efficient High-Resolution Segmented ΣΔ-DAC for Built-In Self-Test Applications," IEEE Transactions on Very Large Scale Integration (TVLSI) Systems, vol. 29, no. 11, pp. 1861-1874, November 2021.

5- **Ahmed S. Emara**, Denis Romanov, Gordon W. Roberts, Sadok Aouini, Mahdi Parvizi and Naim Ben-Hamida, "Optimized Periodic ΣΔ Bitstreams for DC Signal Generation used in Dynamic Calibration Applications," IEEE Open Journal of Circuits and Systems (OJ-CAS), Vol. 1, Issue. 1, pp. 3-12, March 2020.

6- **Ahmed S. Emara**, A. H. Madian, H. H. Amer, S. H. Amer and M. B. Abdelhalim, "On the Production Testing of Memristor Ratioed Logic (MRL) Gates," Circuits and Systems, Scientific Research Publishing, Vol. 7, August 2016, pp. 3016-3025.

Conference Publications

7- J. Guo, **Ahmed S. Emara**, et al., "A 35Tb/s/mm 0.29 pJ/bit 64Gb/s/wire Simultaneous Bidirectional Die-to-Die Interface Transceiver Supporting Independent Reference Clock," accepted for publication in IEEE International Solid-State Circuits Conference (ISSCC), February 2027.

8- Sherif H. Amer, **Ahmed S. Emara**, Hassanein H. Amer, "Method for Yield Enhancement of ReRAM Memory Arrays via Reference Voltage Calibration," proceedings of Nanotechnology Materials and Devices Conference (NMDC), October 2024.

9- Mahmood A. Mohammed, **Ahmed S. Emara**, Gordon W. Roberts, "Slew-Rate Analysis of Scalable Multi-Stage CMOS Operational Transconductance Amplifiers," proceedings of Midwest Symposium on Circuits and Systems (MWSCAS), August 2024.

10- Fekry Y. Mohamed, **Ahmed S. Emara**, Hassanein H. Amer, "Detection of Catastrophic Faults in 6-bit R-2R Ladder DAC," proceedings of International Conference on Electrical, Electronics, and Information Engineering (ICEEIE), September 2023, pp. 1-5.

11- Beatrice Shokry, Hassanein Amer, Ramez Daoud, Mahmoud Rumman and **Ahmed S. Emara**, "Error Detection and Masking Circuit with High Diagnosability for Redundant Sensors," proceedings of Mediterranean Embedded Computing Resources (MECO), June 2023, pp. 1-5.

12- **Ahmed S. Emara**, Gordon W. Roberts, Sadok Aouini, Mahdi Parvizi, and Naim Ben-Hamida, "Using Optimized Butterworth-Based ΣΔ Bitstreams for the Testing of High-Resolution Data Converters," proceedings of New Circuits and Systems (NEWCAS), June 2020, pp. 299-302.

13- **Ahmed S. Emara**, Gordon W. Roberts, Sadok Aouini, Mahdi Parvizi and N. Ben-Hamida, "Selecting the Fastest Settling-Time Filter in PDM-based DACs used for Dynamic Calibration Applications," proceedings of Midwest Symposium on Circuits and Systems (MWSCAS), August 2019, pp. 900-903.

14- **Ahmed S. Emara**, Gordon W. Roberts, Sadok Aouini, Mahdi Parvizi and N. Ben-Hamida, "On the Design of DACs for Dynamic Calibration Applications using Periodic Sequences from ΣΔ Modulators," proceedings of the Circuits, Devices and Systems Symposium of the IEEE Canadian Conference on Electrical and Computer Engineering (CCECE), May 2019, pp. 1-4.

15- **Ahmed S. Emara**, A. H. Madian, H. H. Amer, S. H. Amer, and M. B. Abdelhalim, "Testing of memristor ratioed logic (MRL) XOR gate," proceedings of the International Conference on Microelectronics (ICM), December 2016, pp. 181–184.

16- M. N. Shaker, A. H. Madian, M. B. Abdelhalim, S. H. Amer, **Ahmed S. Emara** and H. H. Amer, "Effect of open faults in FPGA switch matrices on fault detection mechanisms," proceedings of the International Conference on Microelectronics (ICM), December 2016, pp. 233–236.

17- A. Abdulslam, S. H. Amer, **Ahmed S. Emara**, and Y. Ismail, "Evaluation of multi-level buck converters for low-power applications," in proceedings of the International Symposium on Circuits and Systems (ISCAS), May 2016, pp. 794–797.

18- S. H. Amer, A. H. Madian, H. Elsayed and **Ahmed S. Emara**, "Effect of the memristor threshold current on memristor-based Min-Max circuits," proceedings of the International Modern Circuits and Systems Technologies (MOCAST), May 2016, pp. 1-4.

19- **Ahmed S. Emara**, A. H. Madian, H. H. Amer and S. H. Amer, "High Coverage Test for the Second Generation Current Conveyor," proceedings of the International Conference on Electronics, Circuits, and Systems (ICECS), December 2015, pp. 429-432.

20- S. H. Amer, A. H. Madian and **Ahmed S. Emara**, "Design and Analysis of Memristor-based min-max circuit," proceedings of the International Conference on Electronics, Circuits, and Systems (ICECS), December 2015, pp. 187-190.

21- S. H. Amer, A. H. Madian and **Ahmed S. Emara**, "Memristor-based Center-Of-Gravity (COG) defuzzifier circuit," proceedings of the European Conference on Circuit Theory and Design (ECCTD), August 2015, pp. 1-4.

22- R. Mohie Eldin, **Ahmed S. Emara**, S. H. Amer, M. M. Fouad, A. H. Madian, H. H. Amer, M. B. Abdelhalim and H. H. Draz, "Effect of the Resistance of Open and Short Faults on the Production Testing of MCML Gates," proceedings of the Biennial Baltic Electronics Conference (BEC), October 2014, pp. 81-84.

23- S. H. Amer, **Ahmed S. Emara**, R. Mohie-Eldin, M. M. Fouad, A. H. Madian, H. H. Amer, M. B. Abdelhalim and H. H. Draz, "Testing current mode two-input logic gates," proceedings of the Circuits, Devices and Systems Symposium of the IEEE Canadian Conference on Electrical and Computer Engineering (CCECE), May 2014, pp. 1-6.

Teaching Experience

Teaching Assistant, **Electrical and Computer Engineering Dept, McGill University**, Montreal, QC, Canada

- **Mixed-Signal Test Techniques** (ECSE 435): Winter 2020 and Winter 2018
- **Microelectronics** (ECSE 335): Fall 2019
- **Analog Microelectronics** (ECSE 534): Fall 2019
- **Introduction to Electronics** (ECSE 331): Fall 2017

Teaching Assistant, **Electronics and Communications Engineering Dept, AUC**, Cairo, Egypt

- **Testing of Digital Circuits** (ECNG 413/4103): Spring 2016
- **Digital Logic Design** (ECNG 210/2101): Fall 2014, Spring 2015 and Fall 2015

Journal and Conference Activities

- **Executive Editor**, International Journal of Circuit Theory and Application (IJCTA), 2024-Present
- **Technical Program Committee (TPC) Member**, The International Conference on Microelectronics (ICM), 2019-Present.
- **Reviewer,** IEEE Transactions on Circuits and Systems: Express Briefs, 2021